



PATENTS
ALT-283

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION

Applicants : Ramanand Venkata et al.
Application No. : 10/670,845 Confirmation No. : 8303
Filed : September 24, 2003
For : MULTIPLE DATA RATES IN PROGRAMMABLE
LOGIC SERIAL DEVICE INTERFACE
Group Art Unit : 2819

New York, New York 10020
March 25, 2004

Hon. Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. §§ 1.56 and 1.97, applicants hereby make the following patents and publications of record in the above-identified patent application:

Wahlstrom U.S. Patent 3,473,160 (October 14, 1969)
Franaszek et al. U.S. Patent 4,486,739 (December 4,
1984)
Cliff et al. U.S. Patent 5,689,195 (November 18,
1997)
Jeong U.S. Patent 5,802,103 (September 1, 1998)
Cliff et al. U.S. Patent 5,909,126 (June 1, 1999)
Hill U.S. Patent 6,031,428 (February 29, 2000)
Jefferson et al. U.S. Patent 6,215,326 (April 10,
2001)
Schlueter et al. U.S. Patent 6,240,471 (May 29,
2001)
Christopher U.S. Patent 6,270,350 (August 7, 2001)
Silverman et al. U.S. Patent 6,370,603 (April 9,
2002)
Ng U.S. Patent 6,388,591 (May 14, 2002)
Ngai et al. U.S. Patent 6,407,576 (June 18, 2002)



Aung et al. U.S. Patent Application Publication
No. 2001/0033188 A1 (October 25, 2001)
Lee et al. U.S. Patent Application Publication
No. 2002/0190751 A1 (December 19, 2002)
Venkata et al. U.S. Patent Application Publication
No. 2003/0052709 A1 (March 20, 2003)
Andrasic et al. U.S. Patent Application Publication
No. 2003/0155955 A1 (August 21, 2003)

Agere Systems, Inc., "ORCA ORT82G5 0.622/1.0-
1.25/2.0-2.5/3.125 Gbits/s Backplane Interface FPSC,"
Preliminary Data Sheet, pp. 1-35 (July 2001)

Agere Systems, Inc., "ORCA ORT8850 Field-
Programmable System Chip (FPSC) Eight Channel x 850
Mbits/s Backplane Transceiver," Product Brief, pp. 1-6
(July 2001)

Agere Systems, Inc., "ORCA ORT8850 Field-
Programmable System Chip (FPSC) Eight Channel x 850
Mbits/s Backplane Transceiver," Product Brief, pp. 1-36
(August 2001)

Cook, Barry M., "IEEE 1355 Data-Strobe Links: ATM
Speed at RS232 Cost," Microprocessors and Microsystems,
vol. 21, no. 7-8, pp. 421-428 (March 30, 1998)

Electronic Trend Publications, Inc., "Lucent
Introduces 10Gb/s Ethernet FPGAs," Programmable Logic
News and Views, vol. 9, no. 11, pp. 7-8 (November 2000)

Konstas, Jason, "Converting Wide, Parallel Data
Buses to High Speed Serial Links," International IC '99
Conference Proceedings, pp. 19-30 (1991)

Lemme, Helmuth, "Schnelle Chips Für
'Flaschenhälse'," Elektronik, vol. 40, no. 22, pp. 104-
109 (October 29, 1991)

Lucent Technologies, Inc., "Protocol Independent
Gigabit Backplane Transceiver Using Lucent
ORT4622/ORT8850 FPSCs," Application Note, pp. 1-10 (June
2000)

Lucent Technologies, Inc., "ORCA ORT82G5 1.0-
1.25/2.0-2.5/3.125 Gbits/s Backplane Interface FPSC,"
Product Brief, pp. 1-8 (February 2001)

Xilinx, Inc., Virtex-II Pro Platform FPGA Handbook
(UG012 Version 1.0), pp. 1-6, 27-32, 121-126, and 162-
180 (January 31, 2002)



Xilinx, Inc., Rocket I/O Transceiver User Guide
(UG024 Version 1.2), pp. 1-106 (February 25, 2002)

Copies of the aforementioned publications, which are listed on the accompanying Form PTO-1449 (submitted in duplicate), are enclosed herewith.

It is respectfully requested that these publications be (1) fully considered by the Patent and Trademark Office during examination of this application; and (2) printed on any patent which may issue on this application. Applicants request that a copy of Form PTO-1449, as considered and initialled by the Examiner, be returned with the next communication.

Applicants further make the following pending United States patent applications, of which copies are enclosed, of record in the above-identified patent application:

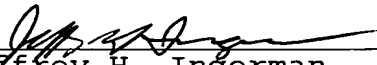
Lee et al. U.S. Patent Application
No. 10/059,014 (January 29, 2002) ✓
Starr et al. U.S. Patent Application
No. 10/209,633 (July 30, 2002) ✓
Venkata et al. U.S. Patent Application
No. 10/273,899 (October 16, 2002) ✓
Venkata et al. U.S. Patent Application
No. 10/317,262 (December 10, 2002) ✓
Venkata et al. U.S. Patent Application
No. 10/317,264 (December 10, 2002)
Venkata et al. U.S. Patent Application
No. 10/349,541 (January 21, 2003) ✓
Lui et al. U.S. Patent Application
No. 10/454,626 (June 3, 2003) ✓

It is respectfully requested that these applications be fully considered by the Patent and Trademark Office during the examination of the above-captioned patent application.



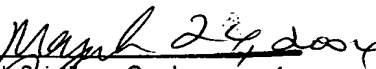
An early and favorable action is respectfully requested.

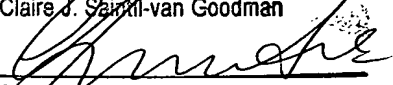
Respectfully submitted,



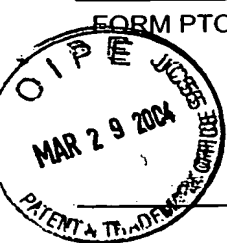
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U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEINFORMATION DISCLOSURE
STATEMENT BY APPLICANTSATTY. DOCKET NO.
ALT-283APPLN. NO.
10/670,845APPLICANTS
Ramanand Venkata et al.CONF. NO.
8303FILING DATE
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2819

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	3,473,160	10/1969	Wahlstrom	326	41	
	4,486,739	12/1984	Franaszek et al.	341	59	
	5,689,195	11/1997	Cliff et al.	326	41	
	5,802,103	9/1998	Jeong	375	220	
	5,909,126	6/1999	Cliff et al.	326	41	
	6,031,428	2/2000	Hill	331	11	
	6,215,326	4/2001	Jefferson et al.	326	41	
	6,240,471	5/2001	Schlueter et al.	710	62	
	6,270,350	8/2001	Christopher	434	69	
	6,370,603	4/2002	Silverman et al.	710	72	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER INITIAL	
✓	Agere Systems, Inc., "ORCA ORT82G5 1.0-1.25/2.0-2.5/3.125 Gbits/s Backplane Interface FPSC," Preliminary Data Sheet, pp. 1-35 (July 2001)
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✓	Cook, Barry M., "IEEE 1355 Data-Strobe Links: ATM Speed at RS232 Cost," <u>Microprocessors and Microsystems</u> , vol. 21, no. 7-8, pp. 421-428 (March 30, 1998)
✓	Electronic Trend Publications, Inc., "Lucent Introduces 10Gb/s Ethernet FPGAs," <u>Programmable Logic News and Views</u> , vol. 9, no. 11, pp. 7-8 (November 2000)

EXAMINER

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	6,388,591	5/2002	Ng	341	100	
	6,407,576	6/2002	Ngai et al.	326	41	
	2001/0033188 A1	10/2001	Aung et al.	327	41	
	2002/0190751 A1	12/2002	Lee et al.	326	39	
	2003/0052709 A1	3/2003	Venkata et al.	326	37	
	2003/0155955 A1	8/2003	Andrasic et al.	327	277	

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER INITIAL	
/	Konstas, Jason, "Converting Wide, Parallel Data Buses to High Speed Serial Links," <u>International IC '99 Conference Proceedings</u> , pp. 19-30 (1991)
/	Lemme, Helmut, "Schnelle Chips Für 'Flaschenhalse'," <u>Elektronik</u> , vol. 40, no. 22, pp. 104-109 (October 29, 1991)
/	Lucent Technologies, Inc., "Protocol Independent Gigabit Backplane Transceiver Using Lucent ORT4622/ORT8850 FPSCs," Application Note, pp. 1-10 (June 2000)
/	Lucent Technologies, Inc., "ORCA ORT82G5 0.622/1.0-1.25/2.0-2.5/3.125 Gbits/s Backplane Interface FPSC," Product Brief, pp. 1-8 (February 2001)
/	Xilinx, Inc., <u>Virtex-II Pro Platform FPGA Handbook</u> (UG012 Version 1.0), pp. 1-6, 27-32, 121-126, and 162-180 (January 31, 2002)
/	Xilinx, Inc., <u>Rocket I/O Transceiver User Guide</u> (UG024 Version 1.2), pp. 1-106 (February 25, 2002)

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